REMARKS

Claim 11 is canceled; claims 9 and 20 are amended; and claims 1-10 and 12-20 are pending in the application. The application is amended to correct a minor typographical error at line 19 of page 9.

Claim 20 stands objected to for containing a spelling error. Specifically, the Examiner contends that "to" should be changed to "two". Applicant thanks the Examiner for the careful reading of the claims, and has amended claim 20 to correct the spelling error. Applicant requests that the Examiner's objection to claim 20 be withdrawn in the Examiner's next action.

Claims 1-8 stand rejected as being unpatentable over Tsukamoto in view of Parekh. Applicant requests reconsideration of such rejections.

Referring initially to claim 1, such recites a method wherein a conductive structure is formed over a substrate, and wherein an electrically insulative material is formed along at least a portion of the conductive structure. The claim recites that the electrically insulative material comprises at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10. Additionally, the claim recites that a dopant barrier layer is formed over the electrically insulative material, and that a doped oxide material is formed over the dopant barrier layer. Further, the claim recites that the dopant barrier layer prevents dopant migration from the doped oxide material to the electrically insulative material.

The Examiner contends that the various recited features of claim 1 can be found within the combination of Tsukamoto and Parekh. Specifically, the

Examiner contends that the recited formation of an electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q can be found in Tsukamoto, and the recited formation of a dopant barrier layer over an electrically insulative material can be found in Parekh. Applicant notes, however, that the dopant barrier layer of Parekh (an oxide layer 32a in Parekh's Fig. 6) is formed over an insulative material comprising nitride (spacers 30a of Fig. 6), and further that there is no disclosure or suggestion in Parekh of forming an oxide barrier layer over any material comprising $Si_xO_yN_z$ or Al_pO_q. Applicant further notes that there is no suggestion within Tsukamoto of forming any dopant barrier layer over the disclosed materials comprising $Si_xO_yN_z$ and Al_pO_q.

Applicant submits that the Examiner has failed to establish the requisite criteria for combining Tsukamoto and Parekh in rejecting claim 1, and accordingly requests withdrawal of such rejection in the Examiner's next action.

The Examiner is reminded that under MPEP § 706.02(j) three basic criteria must be met in combining references. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must a reasonable expectation of success; and third, the combined references must teach or suggest all of the limitations of the claims. Also, the teaching or suggestion to make the claimed combination, and the reasonable expectation of success, must both be found in the prior art and not based on applicant's disclosure.

In the present case, the cited references do not teach or suggest all of the limitations of the claims. There is no disclosure within either Tsukamoto or Parekh of a dopant barrier layer over a material comprising $Si_xO_yN_z$ and Al_pO_q.

The Examiner contends it would be obvious to utilize the dopant barrier layer of Parekh relative to the materials of Tsukamoto because Parekh teaches at col. 1, lns. 40-45 that the dopant barrier layer can inhibit the diffusion of phosphorous form an overlying BPSG layer into materials underlying the dopant barrier layer. Applicant submits, however, that Parekh never suggests that a dopant barrier layer should be placed between an overlying BPSG layer and a material comprising $Si_xO_yN_z$ and/or Al_pO_q. Instead, Parekh is recognizing that there can be advantages to utilizing a dopant barrier relative to the insulative materials disclosed therein, and the insulative materials disclosed within Parekh do not include $Si_xO_yN_z$ and/or Al_pO_q.

The Examiner's other cited reference of Tsukamoto discloses utilization of layers comprising $Si_xO_yN_z$ and/or Al_pO_q without utilization of any dopant barrier. There is accordingly no teaching of a dopant barrier layer over $Si_xO_yN_z$ and/or Al_pO_q within Tsukamoto. To the extent anything can be inferred from Tsukamoto about utilization of barrier layers over $Si_xO_yN_z$ and/or Al_pO_q, it is that a dopant barrier layer is unnecessary relative to $Si_xO_yN_z$ and/or Al_pO_q.

As neither of the Examiner's cited references contains any teaching or suggestion of a dopant barrier layer utilized over $Si_xO_yN_z$ and/or Al_pO_q, and as one of the references specifically describes $Si_xO_yN_z$ and/or Al_pO_q utilized without a dopant barrier layer, it is inconceivable that the combined references can be

considered to teach the claim 1 recited feature of a barrier layer formed over $Si_xO_yN_z$ and/or Al_pO_q. Applicant therefore requests formal allowance of claim 1 in the Examiner's next action.

Claims 2-8 depend from claim 1, and are therefore allowable for at least the reasons discussed above regarding claim 1.

Referring next to claims 14-18, such claims, like the above-referenced claim 1, stand rejected as being unpatentable over Tsukamoto and Parekh. Applicant requests reconsideration of such rejections.

Referring to claim 14, such claim recites a method wherein a silicon oxide is chemical vapor deposited over an electrically insulative material comprising $Si_xO_yN_z$ and/or Al_pO_q, and wherein BPSG is subsequently formed over the silicon oxide. Applicant's specification explains at page 11, lns. 8-20 that the silicon oxide formed by chemical vapor deposition, and placed between BPSG and an insulative material comprising $Si_xO_yN_z$ and/or Al_pO_q, can be considered a dopant barrier layer which prevents dopant migration from the BPSG to the underlying $Si_xO_yN_z$ and/or Al_pO_q. Accordingly, claim 14 is allowable for reasons similar to those discussed above regarding claim 1, and application requests such allowance in the Examiner's next action.

Claims 15-18 depend from claim 14, and are therefore allowable for at least the reasons discussed above regarding claim 14. Applicant therefore requests allowance of claims 15-18 in the Examiner's next action.

Referring to claim 9, such stands rejected over Fu. Claim 9 is amended to recite a method wherein an electrically insulative material is formed along an

lectrically conductive material of a transistor gat sidewall, and further wherein the electrically insulative material comprises two separate layers, with one of the layers being closest to the transistor gate sidewall and comprising $Si_xO_yN_z$ and/or Al_pO_q, and the other layer being further from the gate sidewall and consisting essentially of silicon and nitrogen.

Fu discloses methods wherein a pair of insulative materials are formed along a transistor gate sidewall, and wherein one of the layers comprises silicon nitride, and the other comprises silicon oxynitride. However, applicant notes that Fu only discloses applications in which the layer comprising silicon nitride is along the transistor gate sidewall, and the layer comprising silicon oxynitride is further from the transistor gate sidewall than the layer comprising silicon nitride. In other words, Fu discloses exactly the opposite arrangement of the insulative layers as is recited in claim 9: Whereas claim 9 recites the silicon nitride being <u>further</u> from the transistor gate sidewall than the $Si_xO_yN_z$, Fu discloses that the silicon nitride is <u>nearer</u> the gate sidewall than the silicon oxynitride. There is no suggestion within Fu of reversing the order of the two layers disclosed in Fu, and accordingly there is no suggestion of the claim 9 recited structure. Additionally, applicant submits that page 12, lns. 9-16 of Applicant's specification describes a specific advantage for having a layer closest to a transistor sidewall (referred to as an innermost layer on page 12) contain $Si_xO_yN_z$, and the layer further from the transistor gate sidewall (referred to on page 12 as the outermost layer) consist of silicon nitride. The advantage is that if some over-etching occurs during a SAC etch, it will be the silicon nitride layer which is removed

rather than the layer containing $Si_xO_yN_z$. Such is xactly the opposite of the embodiment of Fu. It is inconceivable that a reference that teaches exactly the opposite of the claim 9 recited method could be considered to suggest the claim 9 recited method. For at least this reason claim 9 is allowable over Fu, and applicant therefore requests such allowance in the Examiner's next action.

Claims 10, 12 and 13 depend from claim 9, and are therefore allowable for at least the reasons discussed above regarding claim 9. Applicant therefore requests formal allowance of claims 10, 12 and 13 in the Examiner's next action.

Referring next to claim 19, such stands rejected as being unpatentable over a combination of Fu and Parekh. Claim 19 recites a method wherein a silicon oxide layer is formed over a material comprising $Si_xO_yN_z$ and/or Al_pO_q, and subsequently BPSG is formed over the silicon oxide. Accordingly, claim 19 recites a method wherein a dopant barrier layer is formed between BPSG and a material comprising $Si_xO_yN_z$ and/or Al_pO_q.

The Examiner recognizes that neither Fu nor Parekh specifically discloses forming a dopant barrier layer over a material comprising $Si_xO_yN_z$ and/or Al_pO_q, but contends similarly to the contention utilized in rejecting claim 1 that it would be obvious to utilize the dopant barrier layer of Parekh over a material comprising $Si_xO_yN_z$ and/or Al_pO_q. However, as argued above relative to claim 1, the Examiner's contention is mistaken, and applicant's recited utilization of a dopant barrier layer between a doped material and a material comprising $Si_xO_yN_z$ and/or Al_pO_q is not obvious relative to the teachings of Parekh, or relative to any combination of th t achings of Parekh with references simply disclosing that

materials comprising $Si_xO_yN_z$ and/or Al_pO_q are known. Missing from such combinations is any suggestion that there would be a reason or advantage to forming a dopant barrier layer over the material comprising $Si_xO_yN_z$ and/or Al_pO_q. Further, applicant has provided in the specification a specific reason for providing a dopant barrier layer relative to insulative materials comprising $Si_xO_yN_z$ and/or Al_pO_q, which is, as explained at page 11, lns. 14-20, that the barrier layer can alleviate problems with dopant migrating into $Si_xO_yN_z$ and/or Al_pO_q, and changing such materials from being insulative materials to being electrically conductive.

Claim 19 is allowable over the combination of Fu and Parekh for the reasons discussed above, and applicant therefore requests formal allowance of claim 19 in the Examiner's next action.

Claim 20 depends from claim 19, and is therefore allowable for at least the reasons discussed above regarding claim 19. Applicant therefore requests formal allowance of claim 20 in the Examiner's next action.

Claims 1-10 and 12-20 are allowable for the reasons discussed above, and applicant therefore requests that the Examiner's next action be a Notice of Allowance formally allowing claims 1-10 and 12-20.

Respectfully submitted,

Dated: 4/10/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/651,422
Filing Date ..... August 30, 2000
Inventor ..... Jeffrey W. Honeycutt et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2815
Examiner ..... A. Wilson
Attorney's Docket No. MI22-1332
Title: Methods of Forming Insulative Material Against Conductive Structures

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO FEBRUARY 7, 2002 OFFICE ACTION

In the Specification

The title is amended as follows:

~~Transistor Structures, Methods of Forming Transistor Structures, and~~ Methods of Forming Insulative Material Against Conductive Structures

The paragraph beginning at p. 9, ln. 8 is amended as follows:

In particular embodiments, one of layers 42 and 44 can consist of either $Si_xO_yN_z$ or Al_pO_q (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of silicon and nitrogen), and can be, for example, Si_3N_4. Alternatively, one of layers 42 and 44 can consist of aluminum and oxygen (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of such materials). In yet another alternative embodiment,

one of layers 42 and 44 can consist of silicon, nitrogen and oxygen (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of such materials). An exemplary material which consists of aluminum and oxygen is Al_2O_3.

In the Claims

Cancel claim 11.

9. (Amended) A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers; the at least two layers having different chemical compositions from one another; a first of the at least two layers comprising at least one of $Si_xO_yN_z$ or Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10; a second of the at least two layers consisting essentially of silicon and nitrogen; and

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall; the anisotropically etching comprising etching both of the first and second of the at least two layers; and

wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall.

20. (amended) The method of claim 19 wherein the electrically insulative material comprises ~~to~~ two different layers that are against one another, one of the two layers consisting of silicon nitride, and the other of the two layers consisting of either the $Si_xO_yN_z$ or the Al_pO_q.

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